

REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

Claims 1-3 and 10-11 stand rejected under 35 U.S.C. § 102(e) [103(a)?] based on each of Katagiri et al. (US Patent 6841881) and Kado et al. (US Patent 7042073) in view of Lin et al. (US Patent 6359340). Claims 1-3 and 6-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiroaki et al. (JP2001-291821) in view of Kanemoto et al. (US Patent 6410987) and further in view of Goller et al. (US Patent 6683374). Applicants respectfully traverse.

In the rejections based on Katagiri and Kado, the Office acknowledged that each of the primary references lacks the feature that the memory chip includes a second plurality of bonding terminals on an upper surface thereof. The rejections rely on Lin for this feature. However, the proposed combination of Lin with the primary references is clearly inappropriate.

Katagiri and Kado disclose a memory chip (2A or 2B) electrically connected to substrate 1 via Au bumps 4, i.e., mounted via the flip-chip method (Katagiri Fig. 2, column 5, lines 1-6; Kado Fig. 2, column 6, lines 12-17). The placement of bonding terminals on the upper surface of such a memory chip is evidently incompatible with the flip-chip

designs taught by the primary references. Accordingly, one skilled in the art would not look to Lin as a basis for modifying Katagiri and Kado in such a manner as would be necessary to produce Applicants' invention. Indeed, such modification is contraindicated by the primary references' flip-chip design. Accordingly, the rejections based on Katagiri and Kado are untenable and should be withdrawn.

Turning to the rejection based on Hiroaki, Kanemoto, and Goller, the Office acknowledged that the principal reference, Hiroaki, fails to disclose that the upper chip and lower chip are the microcomputer chip or the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side [i.e., the second side of the memory chip]. Kanemoto was relied upon as teaching stacked microcomputer and memory chips, but is also deficient with respect to the aforementioned feature of Applicants' invention. Goller fails to supply this deficiency. First of all, In Goller, the square chip is mounted beneath the elongate rectangular chip. Further, and also in contrast to the claimed invention, Goller's elongate rectangular chip lacks bonding terminals along a short side. Further still, Goller's elongate rectangular chip is mounted

by a flip-chip technique, and therefore lacks the claimed bonding terminals on an upper surface thereof

It is therefore apparent that Goller would not have suggested modifying Hiroaki, whether taken with or without Kanemoto, in such a manner as would be necessary to produce Applicants' invention as set forth in Claims 1 and 6.

The rejection based on Hiroaki, Kanemoto, and Goller is accordingly untenable and should be withdrawn.

Independent Claim 14 and dependent Claims 15-20 have been added to provide more comprehensive protection for certain aspects of Applicants' invention. As will be apparent, these claims distinguish patentably from the applied references and should therefore be allowed. Note, for example, that Claim 14 recites that the mounted microcomputer chip covers a portion of each of the two long sides of the memory chip and covers no portion of the first plurality of bonding terminals of the memory chip.

This application is clearly in condition for allowance and should now be passed to issue.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10006) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing

of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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